

# New STMicroelectronics NAND Flash Family for portable consumer equipments and disposable storage media

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STMicroelectronics (NYSE: STM) has completed its 'Small Page' NAND Flash memory roadmap with the introduction of 256-Mbit and 128-Mbit devices to provide cost-effective storage for a range of consumer products that require large amounts of low cost memory. Both of the new devices are available in 3V and 1.8V power supply versions, and they join 512-Mbit and 1-Gbit chips that are already in volume production.

The NAND256 and NAND128 provide ultra-fast data throughput and erase capability, coupled with the low power programming and low voltage operation required by mobile phones, PDAs and other portable equipment. They have been developed using an advanced 120nm

technology, and their small memory cell size ensures that the cost of mass memory is minimized for price-sensitive products, such as consumable low-density storage media, including Flash cards and USB memory sticks.

The Address lines and Data Input/Output signals of all members of the family are multiplexed onto an 8-bit bus, reducing pin count and allowing the use of a modular NAND interface, which enables systems to be modified to use higher (or lower) density devices without changing the footprint.

The new devices are intended to provide cost-effective mass memory for portable consumer equipment such as mobile phones, digital still cameras, PDAs, and GPS navigation systems, disposable low-density Flash cards, consumable USB drives, and removable storage for video games.

A software toolchain available from ST allows fast development of products that use the new memory chips, and can help to extend their useful life. Tools include Error Correction Code (ECC) software; Bad Block Management (BBM) to recognize and replace a block that fails an Erase or Program operation by copying its data to a valid block; Wear Leveling algorithms to optimize the aging of the device by distributing Erase and Program operations among all the blocks; File System OS Native reference software; and hardware simulation models.

The memories are organized into 1024 (NAND128) or 2048 (NAND256) nominal 16 KByte blocks, each of which is divided into pages of 512 Bytes, plus 16 spare bytes per page, that can be read and programmed by page. The spare bytes are typically used for Error Correction Codes, software flags or Bad Block identification. A Copy Back Program mode enables data stored in one page to be programmed directly into another without the need for external buffering, a feature

that is typically used to to move the data if a Page Program operation fails due to a defective block. A Block Erase command is provided, with a block erase time of 2ms. Each block is specified for 100,000 Program and Erase cycles, and 10-year data retention.

Device options include 'Automatic Page 0 Read after Power Up', intended for applications that boot from NAND memory; and 'Chip Enable Don't Care', which simplifies the microcontroller interface and streamlines the use of NAND Flash in combination with other types of memory such as NOR Flash and SRAM - memory combinations are often used where faster devices are needed for code and working memory, while the much lower cost and higher density NAND memory is used for large file storage. A unique device ID can be factory programmed, and a User Programmable Serial number supports increased security in the target application.

The NAND128W3A and NAND256W3A (3V), and the NAND128R3A and NAND256R3A (1.8V), are sampling now. They are available in TSOP48 or VFBGA55 8x10mm ball array packages. Pricing, for 100k units, is US\$5.80 for the 256Mbit product and US\$4.20 for the 128Mbit device.

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