Computer model provides important clues for the production of tightly packed electronic components

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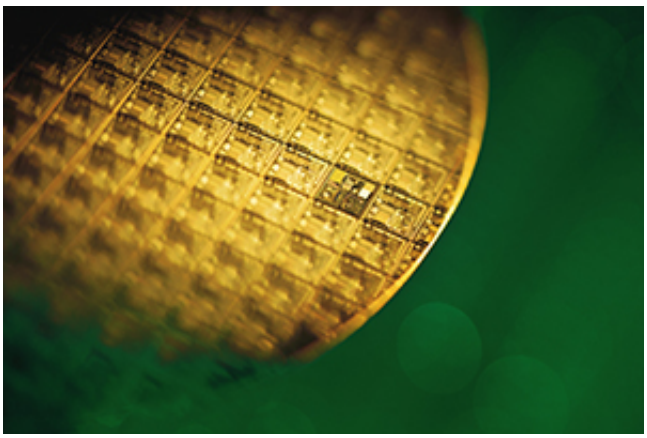

Stacking ever more components on computer chips is aggravating crowding. A computer model developed at A*STAR now allows researchers to predict how a silicon wafer deforms as a consequence. Credit: Comstock/Thinkstock

Greater numbers of ever-smaller components are required to fit on computer chips to meet the ongoing demands of miniaturizing electronic devices. Consequently, computer chips are becoming increasingly crowded. Designers of electronic architectures have therefore followed the lead of urban planners and started to build upward. In so-called 'three-dimensional (3D) packages', for example, several flat, two-dimensional chips can be stacked on top of each other using vertical joints.

Controlling the properties of these complex structures is no easy task, as many factors come into play during production. Faxing Che and Hongyu Li and co-workers from the A*STAR Institute of Microelectronics, Singapore, have now developed a powerful modeling method that allows large-scale simulations—and optimization—of the fabrication process, which provides welcome assistance to designers.

Among the challenges of producing tightly packed computer chips is the need to prevent warpage of the underlying silicon wafer as electronics components are stacked on it (see image). Warpage leads to a number of unwanted effects. "Strong warpage can cause wafer breakage, it makes tight packing more difficult and some processing machines cannot handle high-warpage wafers," explains Li. The degree of warpage depends on many design and process parameters, and optimizing the procedure experimentally is time-consuming and costly.

Using their computer model, Che and Li studied a wide range of parameters that influence the warpage of an 8-inch diameter silicon wafer. They focused, in particular, on how a silicon substrate responds to the deposition of layers of copper—through which electrical currents eventually flow. "This is the first time that a model has been … able to predict warpage [at] the level of the entire wafer," says Li. Moreover, the stress on the wafer can be determined accurately. The calculated values agreed well with experimental data. Importantly, with the computer simulations, the researchers could explore regimes that cannot be easily studied experimentally, such as how the depth of the connections between layers influences wafer warpage.

The next goal is to simulate even larger wafers with variable connection sizes, explains Li. "Today, there are two industry standards for 3D packaging applications, 8-inch and 12-inch wafers, but the latter are becoming increasingly important," she says. The team's model is applicable to these larger wafers, too, but it requires optimization.

Currently, Che, Li and their co-workers are collecting warpage and stress data for 12-inch wafers. They will use these data for developing their model further, according to Li.

More information: Che, F. et al. Development of wafer-level warpage and stress modeling methodology and its application in process optimization for TSV wafers. *IEEE Transactions on Components, Packaging and Manufacturing Technology* 2, 944–955 (2012). ieeexplore.ieee.org/xpl/login. … tp=&arnumber=6189753

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