SEMATECH Achieves Submicron 3D IC Bond Alignment Results in Integrated Bonding Tool Platform

June 10 2010

Researchers from SEMATECH's 3D Interconnect program based at the College of Nanoscale Science and Engineering's (CNSE) Albany NanoTech Complex have reported advances in wafer-to-wafer bonding alignment accuracies through a series of tool and process hardening improvements.

At the same time, the SEMATECH team has explored unique 3D metrology and failure analysis techniques to complement bonding tool development. These results are key steps towards bridging high-volume manufacturing readiness gaps for an integrated bonding tool platform and developing metrology techniques that will accelerate adoption of 3D integration technology.

SEMATECH presented the results at the 2010 IEEE International Interconnect Technology Conference (IITC) on Wednesday, June 9, in Burlingame, CA.

Wafer-to-wafer (WtW) alignment and bonding are key enabling process steps for 3D interconnection of wafers through stacking. The International Technology Roadmap for Semiconductors (ITRS) roadmap for high density, intermediate level, through-silicon-vias with WtW bonding specifies via diameters of 0.8 to 1.5µm in 2012 and beyond. Post bond overlay accuracy of 0.5 to 1.0µm is necessary for these devices.

SEMATECH's 3D interconnect researchers have demonstrated submicron alignment accuracies for copper-to-copper (Cu-Cu) thermo-compression bonds and a variety of silicon-to-silicon and oxide-to-oxide fusion bonds without sacrificing bonding uniformity and bonding strength, using an integrated 300mm WtW pre-processing, aligning, and bonding tool. Additionally, to enhance process control, related metrology development on bonding interface defectivity and overlay metrology were reported. SEMATECH's latest achievements are promising indications of the feasibility of meeting the WtW bonding roadmap as outlined in the ITRS.

"Through collaborative research, our goal is to develop and characterize new approaches to implementing 3D," said Sitaram Arkalgud, director of SEMATECH's 3D Interconnect Program. "These leading-edge results, which have a direct impact on processing costs, demonstrate SEMATECH's leadership and innovative techniques that pave the way for low-cost 3D IC integration."

With the rising demand for smaller, more functional and lower-power chips, 3D architecture is emerging as a leading solution for meeting leading-edge consumer device requirements. SEMATECH's 3D program was established at CNSE's Albany NanoTech Complex to deliver robust 300 mm equipment and process technology solutions for high-volume through-silicon via (TSV) manufacturing.

To accelerate progress in realizing 3D's potential as a manufacturable and affordable technology for memory and CMOS manufacturers, the program's engineers have been working jointly with chipmakers, equipment and materials suppliers, and assembly and packaging service companies from around the world on early development challenges, including cost modeling, technology option narrowing, and technology development and benchmarking.

Provided by College of Nanoscale Science and Engineering